EDGEWOOD
CHEMICAL BIOLOGICAL CENTER
U.S. ARMY SOLDIER AND BIOLOGICAL CHEMICAL COMMAND

ECBC-TR-095

FREQUENCY AGILE LASER (FAL) LIDAR TRIGGER AND SIGNAL SIMULATOR TEST SET

Raphael P. Moon

RESEARCH AND TECHNOLOGY DIRECTORATE

July 2000

Approved for public release;
distribution in unlimited.

Aberdeen Proving Ground, MD 21010-5424

20000804 170

Disclaimer

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorizing documents.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY *(Leave Blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	July 2000	Final; 99 Sep - 00 Apr

4. TITLE AND SUBTITLE
Frequency Agile Laser (FAL) LIDAR Trigger and Signal Simulator Test Set

5. FUNDING NUMBERS
PR-20140/CB2

6. AUTHOR(S)
Moon, Raphael P.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
DIR, ECBC, ATTN: AMSSB-RRT-DL, APG, MD 21010-5424

8. PERFORMING ORGANIZATION REPORT NUMBER
ECBC-TR-095

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

Frequency Agile CO_2 laser (FAL) is a laser-based standoff chemical sensor that was developed by Hughes Aircraft Company for ECBC. This document describes detailed design of the FAL LIDAR trigger and signal simulator test set. The test set provides burst trigger pulses, 12 laser trigger pulses, and 15 unique LIDAR return signals at 1 km. One return signal output provides peak signal amplitudes of 18 mV to 1.8 V, and the second provides output of 54 mV to 5.4 V. Purpose of this test set eliminates the need for operating the laser during hardware and software evaluation of data acquisition system.

14. SUBJECT TERMS
FAL LIDAR LASER
Frequency Agile Simulator

15. NUMBER OF PAGES
37

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	**UNCLASSIFIED**	**UNCLASSIFIED**	**UL**

Blank

PREFACE

The work described in this report was authorized under Project No. 20140/CB2, Exploratory Development. The work was started in September 1999 and completed in April 2000.

The use of either trade or manufacturers' names in this report does not constitute an official endorsement of any commercial products. This report may not be cited for purposes of advertisement.

This report has been approved for public release. Registered users should request additional copies from the Defense Technical Information Center; unregistered users should direct such requests to the National Technical Information Service.

Acknowledgments

The author would like to thank Norman Green, Science and Technology Corporation, whose electronic design contributed significantly to this work.

Blank

CONTENTS

FIGURES

TABLE

FREQUENCY AGILE LASER (FAL) LIDAR TRIGGER AND SIGNAL SIMULATOR TEST SET

1. BACKGROUND

The FAL sensor is a Light Detection and Ranging (LIDAR) transceiver. Such a transceiver uses a laser as a transmitter and an optical telescope/detector assembly for a receiver. The signal trigger sources originate on the lidar optical system and consist of the following:

- Laser Trigger (LT) – It is synchronized with the laser high voltage discharge that generates an output laser pulse. The LT signal is used to electronically trigger the data acquisition system every time a laser pulse is fired. It typically precedes the laser output by 1-2 μs.

- Burst Trigger (BT) - It is a marker pulse used to synchronize ordered patterns of laser wavelengths. This timing pulse is coincident with Laser Trigger (LT) for the first laser pulse in the wavelength pattern. The BT pulse is used to arm the data acquisition system.

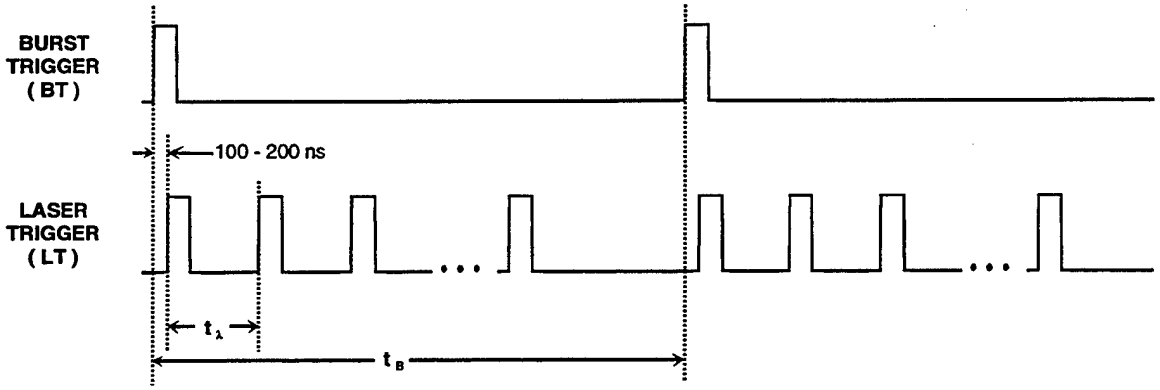


Figure 1. Frequency agile laser timing diagram.

Operation of the FAL is performed by repeatedly transmitting a pre-programmed pattern of laser wavelengths in a pulse burst sequence as shown in Figure 2. The number of wavelengths in a pattern, N, can be variable up to 20, the total amount of available wavelengths for the FAL laser. The spacing between wavelengths, τ_λ, is 5 ms for the FAL.. The burst spacing, τ_B, is dependent upon the number of wavelengths in a pattern and the duty cycle of the laser. We will refer to the burst repetition frequency (BRF) as the rate at which a burst is repeated. The pulse repetition frequency (PRF) will refer to the wavelength spacing.

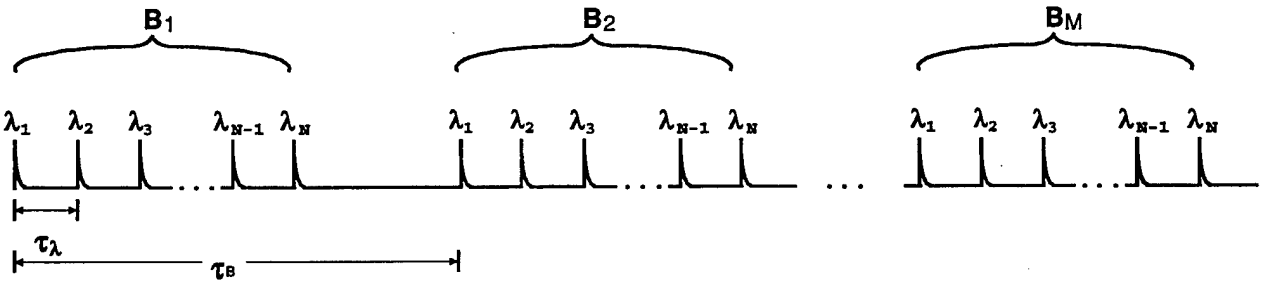


Figure 2. Burst mode operation of frequency agile laser.

Note that when the number of wavelengths in a burst is reduced to N=1, the FAL operates as a normal single-frequency laser, and BRF = PRF. This is a mode of operation that can be applied for target location, target tracking, and high PRF cloud mapping applications.

2. TYPICAL FAL LIDAR SIGNAL CHARACTERISTICS

FAL lidar return signals vary in amplitude from noise level to a maximum of 5 volts. Noise is typically from 10 mV to 50 mV peak-to-peak. The signal digitizer has a 3 volt range and is usually set from -300 mV to + 2.7V. Laser transmitted signals are sent in bursts of 1 to 20 pulses, varying in wavelength from 9.2 to 10.7 μm. PRF is 200 Hz. Burst rate is typically 1Hz. Laser return signals may vary in amplitude from pulse to pulse determined by target characteristics. Signal amplitudes greater than 3 volts will result in signal distortion due to waveform clipping. Small signals just above the noise level will be digitized with reduced accuracy due to digitizer resolution limitations.

Although manual signal amplifier gain adjustments may be employed, field experience has shown that signal amplitudes frequently vary more quickly than an operator can compensate, resulting in a high percentage of distorted data.

3. LIDAR SIMULATOR TEST SET

Figure 3 is a timing diagram showing waveforms generated by the lidar simulator test set. Those waveforms represent Burst Trigger and Laser Trigger pulses, as well as target return signals of the FAL. Target range, as illustrated in the timing diagram, is 1 km (6.67 μs), however, a front panel switch allows range setting of either 1 or 5 km.

Figure 4 is a front panel view of the test set. There are two signal output BNC connectors. One output provides peak signal amplitudes of 18 mV to 1.8 V and the second output, 54 mV to 5.4 V. The Burst Trigger and Laser Trigger pulses are available at front panel BNC connectors. Sixteen test points provide oscilloscope-synchronizing pulses to allow oscilloscope observation of individual test and output signal waveforms.

4. DETAILED DESIGN

Figure 5 is an electrical schematic diagram of the lidar simulator test set. Fifteen simulated lidar return signals are generated following the 15 laser trigger pulses. (Refer to figure 3.) These signals vary sequentially in amplitude from noise level to maximum signal level.

Circuit timing is controlled by two custom designed field programmable gate array (FPGA) circuits, SUMUL1 and SUMUL2 (See Appendix A). Timing is derived from a 10 MHz crystal controlled clock. SIMUL1 generates the 2 microsecond wide, 1 Hz Burst Trigger pulse, as well as an 800 nanosecond delayed 400 Hz signal required by SUMUL2. A five-bit pre-settable binary counter in SIMUL2 is clocked by the delayed 400 Hz signal. This counter is preset to 31 by the 1 Hz signal from SIMUL1. The least significant bit counter stage triggers a 2μs pulse generator at 100 Hz to produce 15 Laser Trigger pulses as the counter decrements to zero. Outputs from the four most significant stages control binary switch DG406. This switch sequentially connects voltage divider resistors to output D to produce gain control signals for the AD603 voltage controlled amplifier. An 18 millivolt simulated laser return signal is applied to pin 3 of the AD603.

Resistors at the DG406 switch adjust the AD603 control voltage to provide gain from 0 to 40 dB in 15 steps. These data are shown in table 1. Calculated resistor values are theoretical; actual circuit values are the nearest 1% resistor reduced by an assumed 100 ohm switch resistance in the DG406. Amplifier output voltage V varies from 18 mV to 1.8 volts in the

geometric series $V = 0.018 \times 1.3895^N$ for values of N from 0 to 14. Amplifier gain is calculated by the formula, dB gain = 40E+20 where E is the differential input voltage of the AD603 voltage controlled amplifier. Data for the table was calculated using HP Basic program "Resistor.Val". This program may be found in appendix B.

The maximum undistorted output voltage of the AD603 amplifier is approximately 2 volts. In order to provide a 5 volt test signal, an AD846 non-inverting amplifier stage with a volt gain of 3 follows the AD603. The output stage is modified by the addition of a BUF634 amplifier within the feedback loop of the AD846. The BUF634 has adequate drive capability for a 5 volt peak signal into a 50 ohm load. Because the BUF634 is within the feedback loop, its relatively high input offset voltage (±100 mV) is not seen at the output. An additional +5 volt power supply was added in series with the existing +5 volt supply to produce +10 volts for output stage power.

Table. AGC Test Set Resistor Values

AD603 Output Voltage	Control Voltage	Linear Gain	DB Gain	DG 406 Resistor Value	1% Resistor Values (Assuming 100 ohm switch resistance)
.018	0	1	0	1 Meg	1 Meg
.02501	.07143	1.39	2.857	70400	69800
.03475	.1429	1.931	5.714	34700	34800
.4829	.2143	2.683	8.572	22800	22600
.0671	.2857	3.728	11.43	16850	16500
.09323	.3571	5.18	14.29	13280	13000
.1295	.4286	7.197	17.14	10900	10700
.18	.5	10	20	9200	9090
.2501	.5714	13.9	22.86	7925	7870
.3475	.6429	19.31	25.71	6933	6810
.4829	.7143	26.83	28.57	6140	6040
.671	.7857	37.28	31.43	5491	5360
.9323	.8572	51.8	34.29	4950	4870
1.295	.9286	71.97	37.14	4492	4320
1.8	1	100	40	4100	4020

Two signal output terminals are provided. The High Output terminal produces signal amplitudes from 54 millivolts to 5.4 volts. Gain at the low output terminal is reduced by a factor of 3 by means of a 100 ohm resistor in series with the 50 ohm load. The Low Output terminal then produces peak signal amplitudes from 18 millivolts to 1.8 volts.

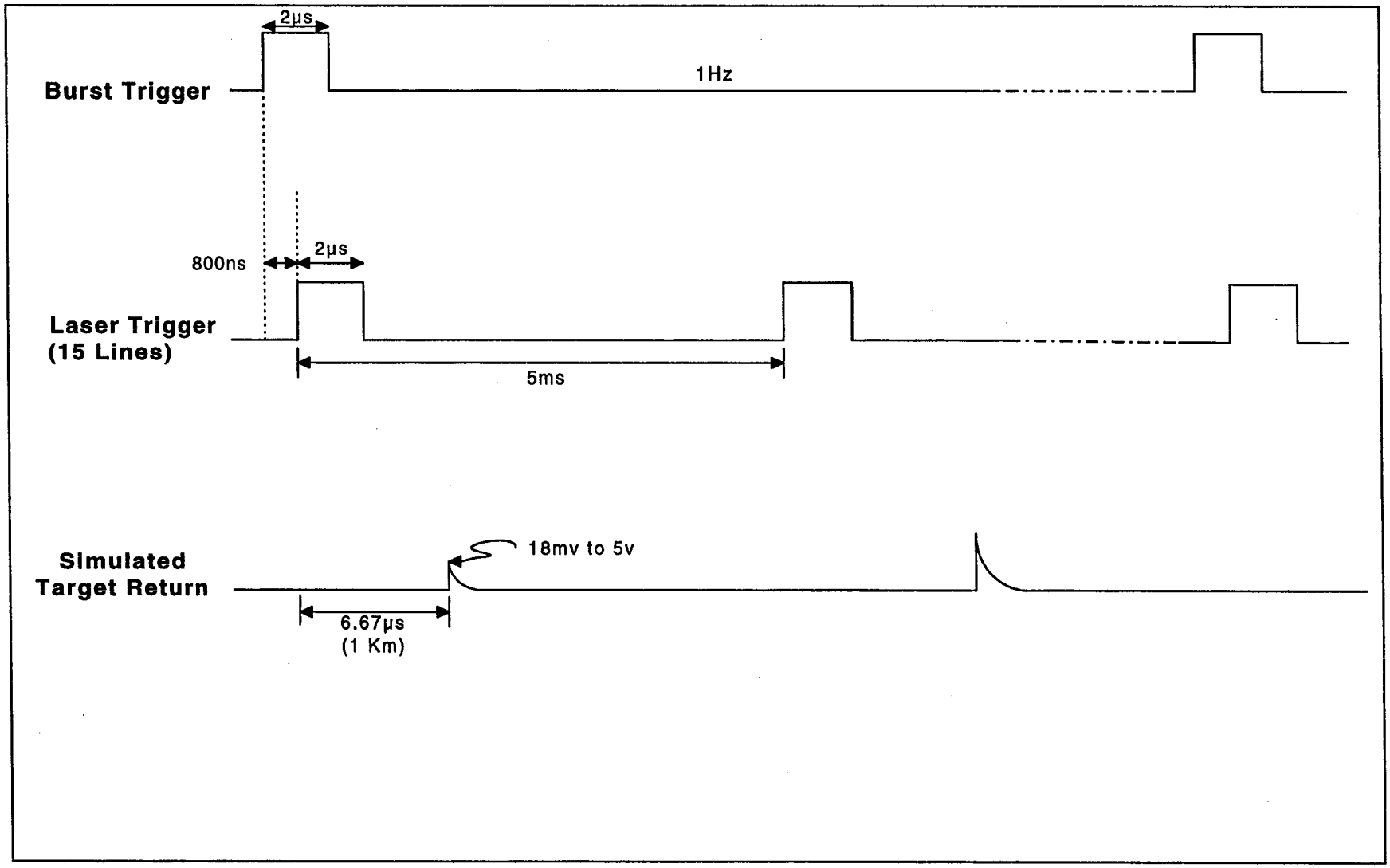


Figure 3. Lidar Simulator test set timing diagram

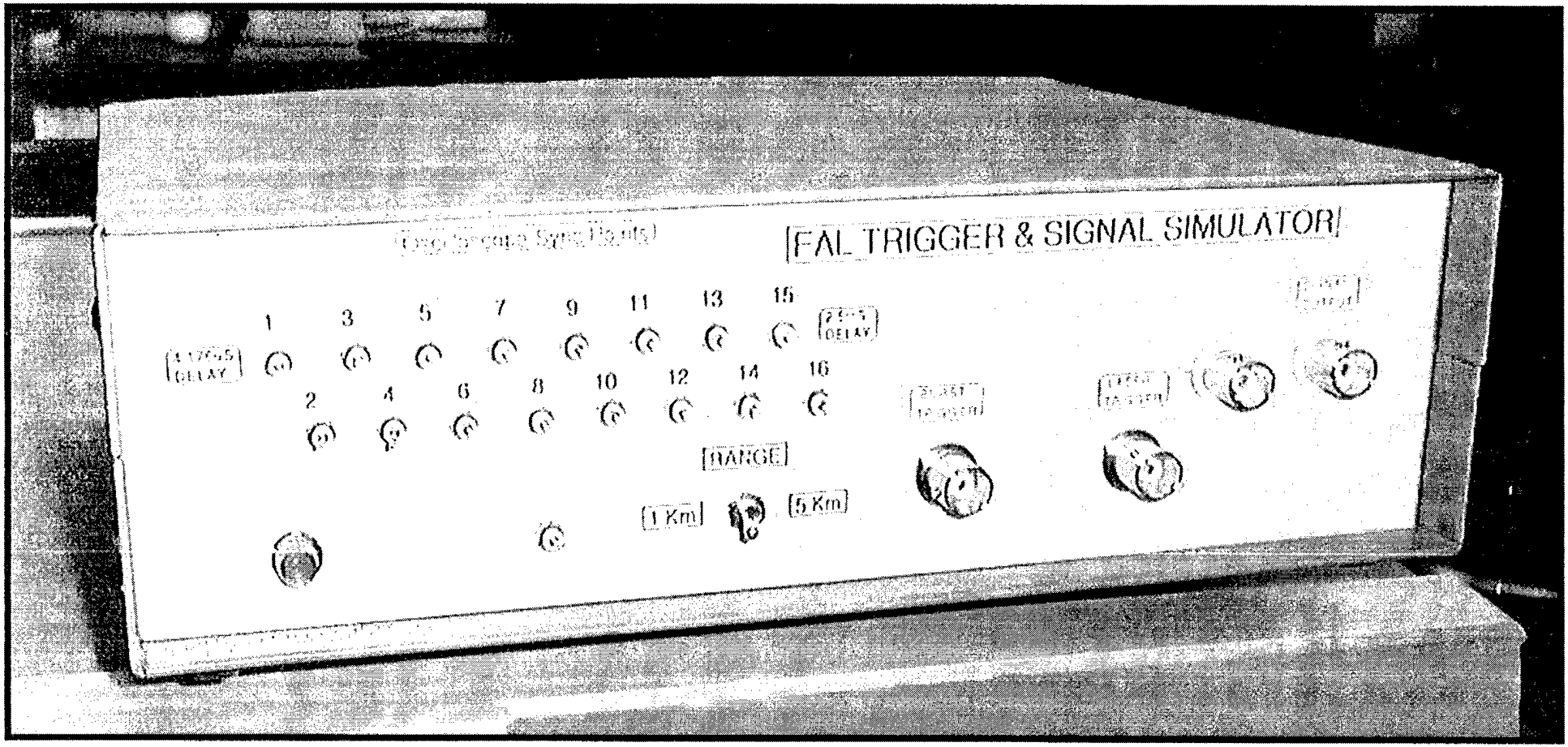


Figure 4. FAL Lidar Simulator test set

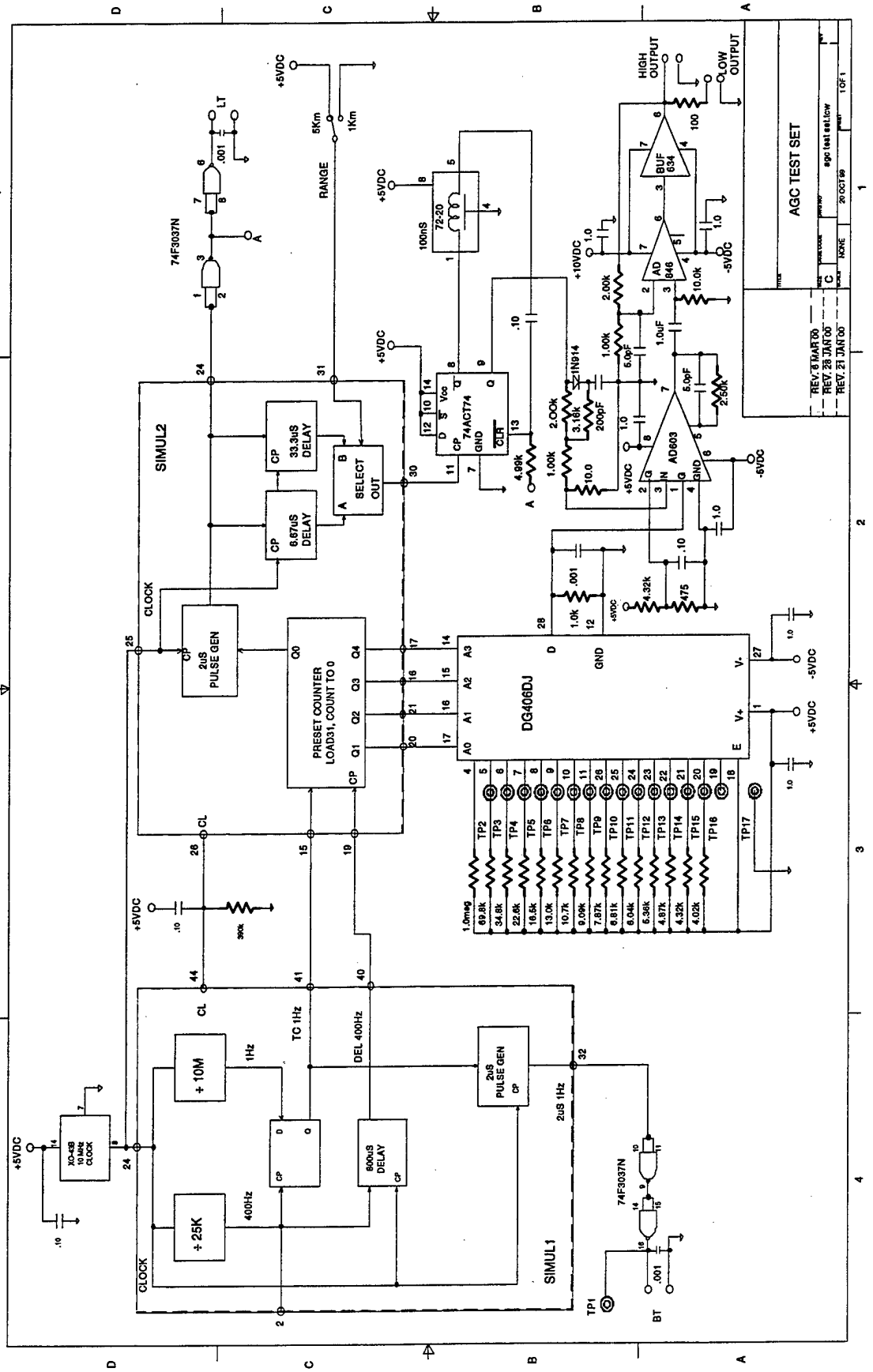


Figure 5. AGC test set schematic

5. OUTPUT SIGNAL WAVEFORM

The test set output signal waveform was synthesized to closely resemble a typical FAL signal. Figure 6 shows the waveform derived from a MICROSIM PSpice circuit analysis of the FAL test set circuit. An oscillograph of an actual FAL signal is included in in-set of figure 6 as a comparison to the synthesized waveform. Figure 7 is a schematic diagram of the circuit used in the PSpice analysis.

Refer to the schematic diagram of figure 7 for the following discussion. The 74ACT74 flip-flop is connected as a delay line monostable multivibrator. A 5 volt 100 ns pulse is generated at the Q output.

The 200 pF capacitor is charged to 5 volts through the 1N914 diode. When the pulse terminates, the 200 pF capacitor discharges though the 3.16K resistor into the voltage divider formed by the 2.00K and the 1.00K resistors. The peak input voltage is reduced to 18 millivolts by the 10 ohm resistor at the AD603 input. The 100 ohm resistor, R34, represents the 100 ohm input impedance of the AD603 amplifier.

6. CONCLUSION

The FAL Lidar simulator test set provides Burst Trigger, 15 Laser Trigger pulses and 15 unique LIDAR return signals at 1 km. This eliminates the need for operating the laser during hardware and software evaluation of the data acquisition system.

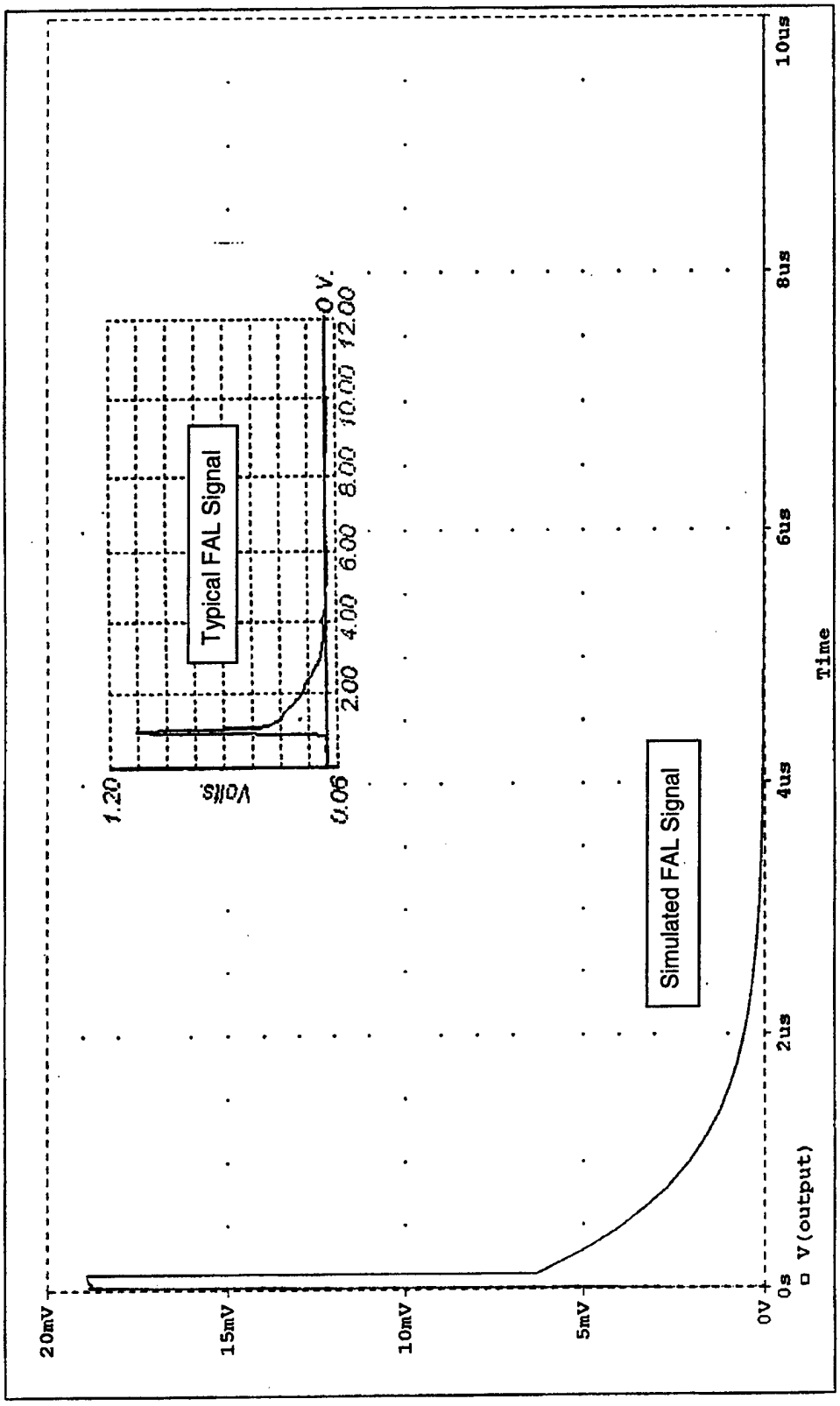


Figure 6. Simulated FAL signal return

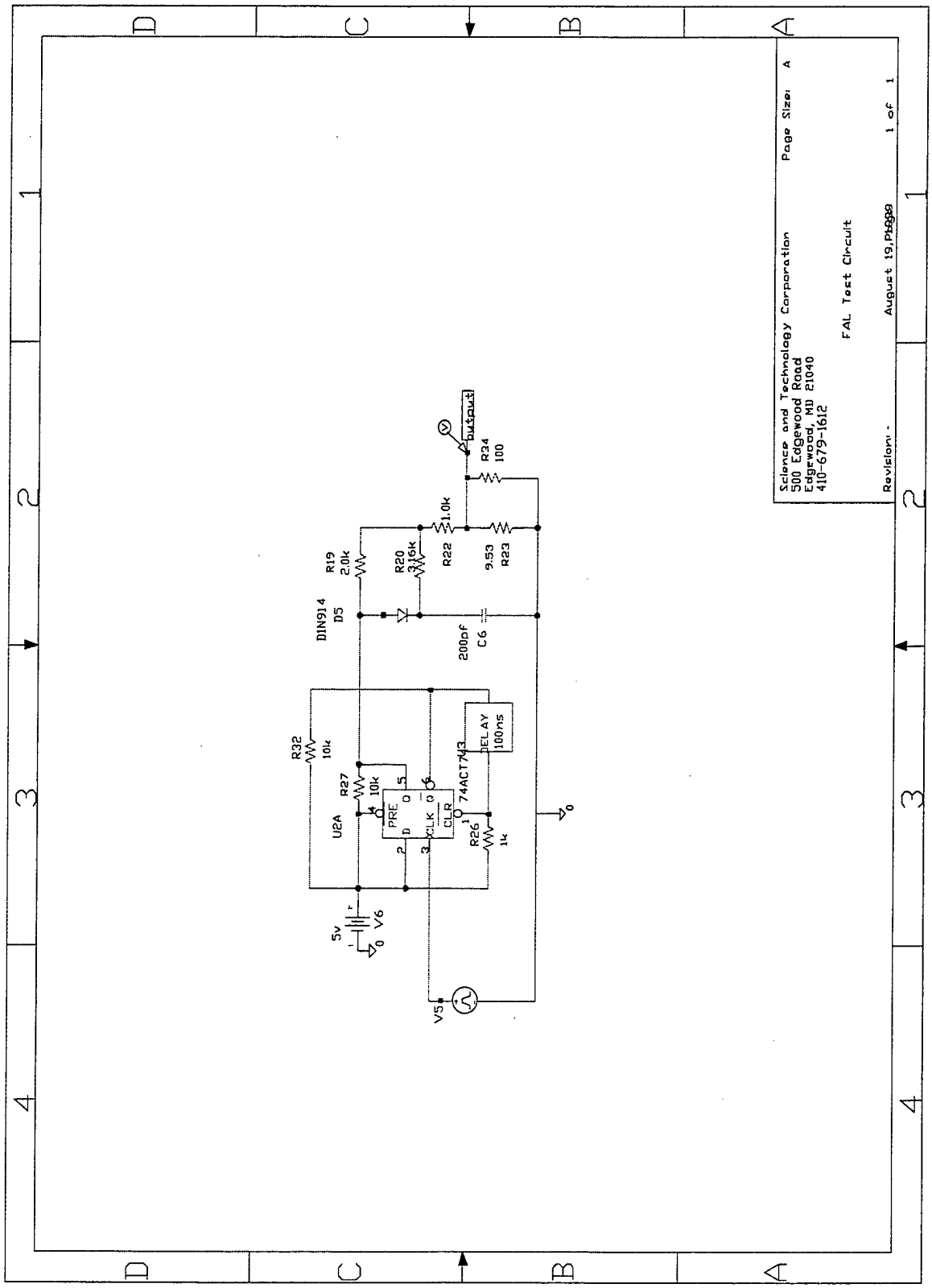


Figure 7. Pulse shaping circuit

Blank

SELECTED REFERENCES

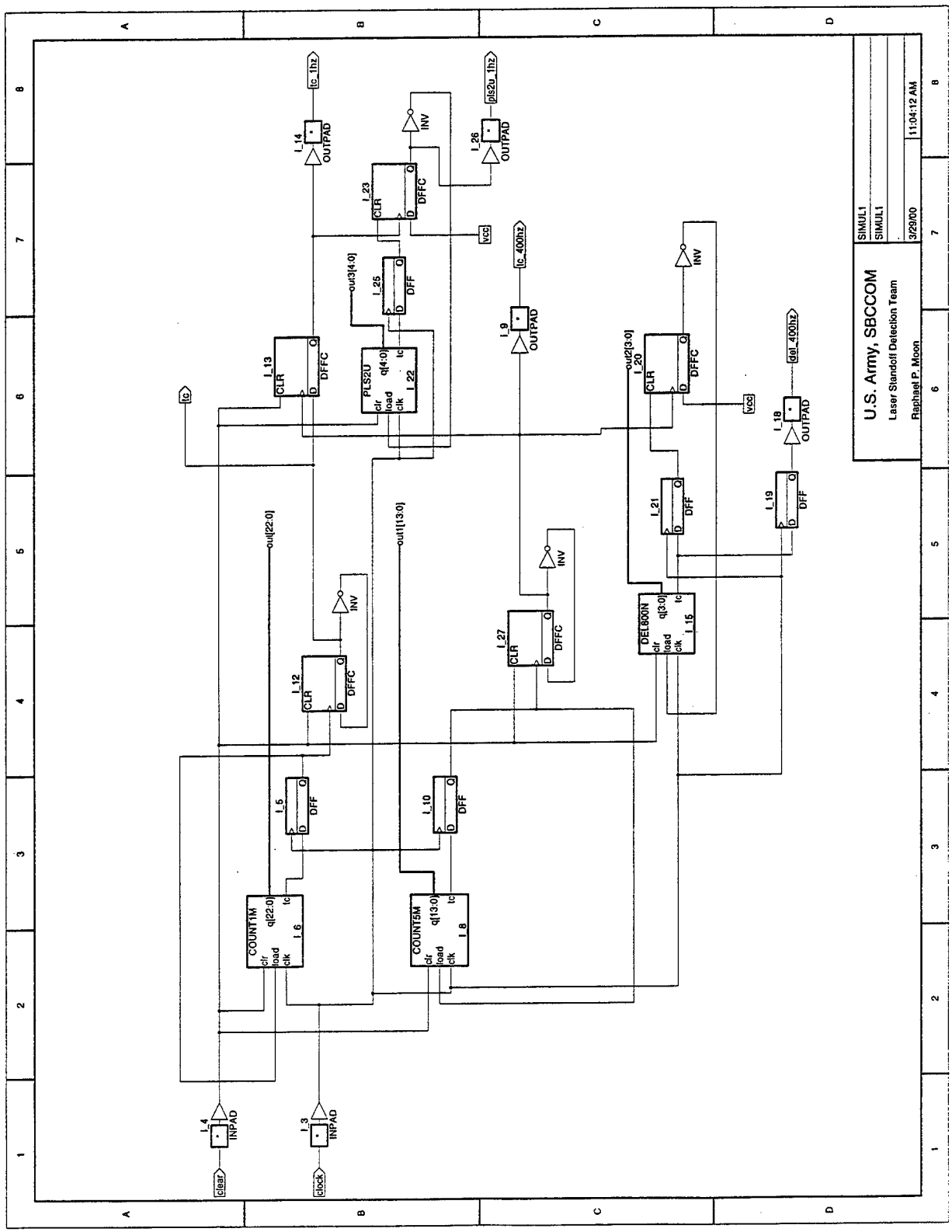
1. WILDCAT Data Acquisition System, F.M. D'Amico, 15 December 1998.

2. STC Technical Report 3241, Norman Green, February 2000.

Blank

APPENDIX A

FIELD PROGRAMMABLE GATE ARRAY (FPGA) CIRCUIT DESIGN USING QUICKLOGIC ASIC (SMUL1 AND SMUL2)


U.S. Army, SBCCOM
Laser Standoff Detection Team
Raphael P. Moon
SIMUL1
SIMUL1
3/29/00
11:04:12 AM
clear
clock
tc
tc_1hz
pls2u_1hz
tc_400hz
del_400hz
vcc
out1[13:0]
out2[3:0]
out3[4:0]
out[22:0]
INPAD
OUTPAD
INV
DFF
DFFC
PLS2U
COUNT1M
COUNT5M
DEL800N

APPENDIX A

```
//--------------------------------------------------------------------------
//
// File name    :  C:\pasic\design\moonwork\lidartest\COUNT5M.v
// Title        :  count5m.v
// Library      :  WORK
//              :
// Purpose      :
//              :
// Created On   : 3/29/00 11:06:45 AM
//              :
// Comments     :
//              :
// Assumptions  : none
// Limitations  : none
// Known Errors : none
// Developers   :
// ------------------------------------------------------------------------
// Revision History :
// ------------------------------------------------------------------------
//   Ver  :| Author           :| Mod. Date :|    Changes Made:
//   v1.0  | Raphael P. Moon  :| 3/29/00   :| Automatically Generated
// ------------------------------------------------------------------------


/*Using 10 Mhz clock,divides down to 800Hz.*/

module count5m(q,load, clk, clr, tc);
output [13:0] q;
output tc;
input load, clk, clr;
reg[13:0] q;
reg tc;

always@(posedge clr or posedge load or posedge clk)
    begin
        if(clr)
            q=14'b11000011010100;
        else
        begin
            if(load)
                q=14'b11000011010100;
            else
                q=q-1;
                    begin
                    if(q==14'b1)
                        tc=1'b1;
                    else
                        tc=1'b0;
                    end
        end
    end
endmodule
```

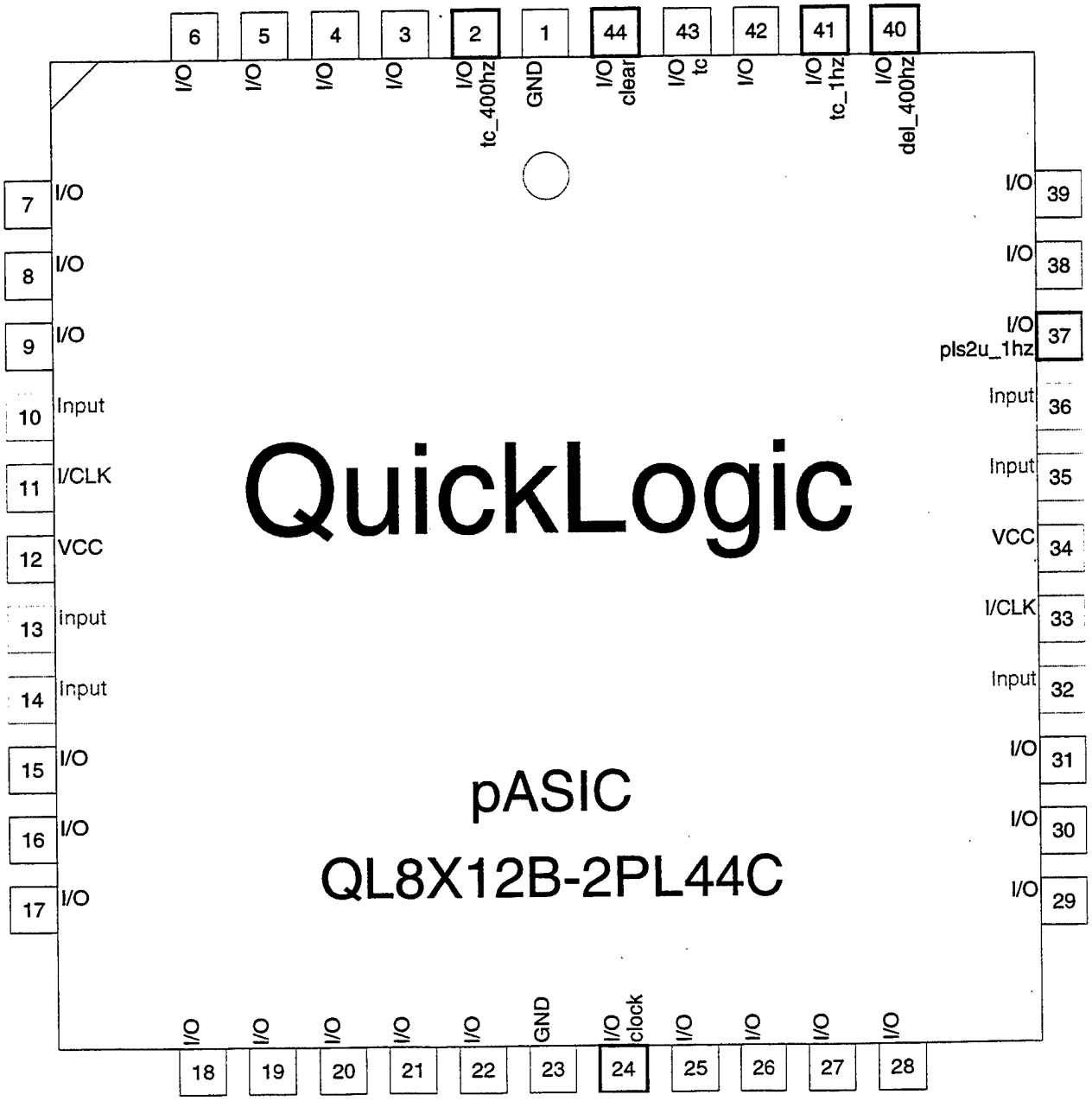
```
//--------------------------------------------------------------------------
//
// File name    :  C:\pasic\design\moonwork\lidartest\COUNT1M.v
// Title        :  count1m.v
// Library      :  WORK
// --------------------------------------------------------------------------
// Revision History :
// --------------------------------------------------------------------------
//   Ver  :| Author            :| Mod. Date :|    Changes Made:
//   v1.0  | Raphael P. Moon   :| 3/29/00   :| Automatically Generated
// --------------------------------------------------------------------------



//Using 10 Mhz clock, divides down to 2Hz.

module count1m(q,load, clk, clr, tc);
output [22:0] q;
output tc;
input load, clk, clr;
reg[22:0] q;
reg tc;

always@(posedge load or posedge clr or posedge clk)
    begin
        if(clr)
            q=23'b10011000100101101000000;
        else
        begin
            if(load)
                q=23'b10011000100101101000000;
            else
                q=q-1;
            begin
                if(q==23'b1)
                    tc=1'b1;
                else
                    tc=1'b0;
            end
        end
    end
endmodule
```

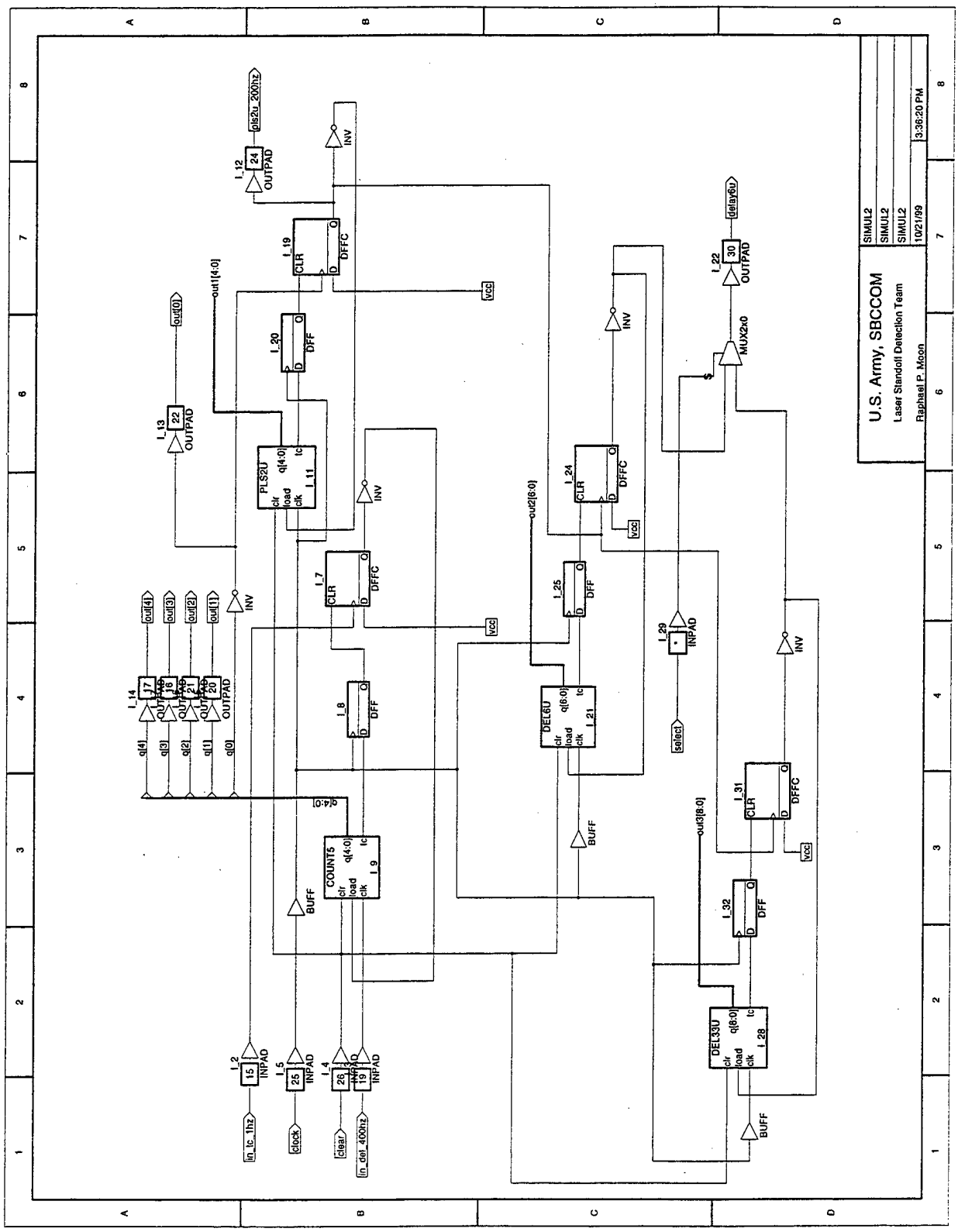
```
//--------------------------------------------------------------------------
//
// File name    :  C:\pasic\design\moonwork\lidartest\DEL800N.v
// ------------------------------------------------------------------------
// Revision History :
// ------------------------------------------------------------------------
//   Ver  :| Author            :| Mod. Date :|    Changes Made:
//   v1.0  | Raphael P. Moon   :| 3/29/00   :| Automatically Generated
// ------------------------------------------------------------------------


/*Using 10 Mhz clock, and 3 bit counter to make 800nsec delay.*/

module del800n(q,load, clk, clr, tc);
output [3:0] q;
output tc;
input load, clk, clr;
reg[3:0] q;
reg tc;

always@(posedge clr or posedge load or posedge clk)
    begin
        if(clr)
            q=4'b1000;
        else
        begin
            if(load)
                q=4'b1000;
            else
                q=q-1;
                    begin
                    if(q==4'b1)
                        tc=1'b1;
                    else
                        tc=1'b0;
                    end
        end
    end
endmodule
```

```
1   //-------------------------------------------------------------------------
    //
    // File name    :  C:\pasic\design\moonwork\lidartest\PLS2U.v
    // ------------------------------------------------------------------------
5   // Revision History :
    // ------------------------------------------------------------------------
    //   Ver  :| Author            :| Mod. Date :|    Changes Made:
    //   v1.0  | Raphael P. Moon   :| 3/29/00   :| Automatically Generated
    // ------------------------------------------------------------------------
10


    /*Using 10 Mhz clock, and 5 bit counter to make 2usec pulse.*/

15  module pls2u(q,load, clk, clr, tc);
    output [4:0] q;
    output tc;
    input load, clk, clr;
    reg[4:0] q;
20  reg tc;

    always@(posedge clr or posedge load or posedge clk)
        begin
            if(clr)
25              q=5'b10100;
            else
            begin
                if(load)
                    q=5'b10100;
30              else
                    q=q-1;
                        begin
                        if(q==5'b1)
                            tc=1'b1;
35                      else
                            tc=1'b0;
                        end
            end
        end
40  endmodule
```

```
1       ++++++++++++++++++++++
        | Design Information |
        ++++++++++++++++++++++
        Design:             simul1
5       SpDE Version:       SpDE 7.11
        Report Generated:   Tue Oct 19 12:03:47 1999
        CHIP Last Updated:  Tue Oct 19 12:03:47 1999
        Part Type:          p8x12b
        Speed Grade:        2
10      Operating Range:    Commercial
        Package Type:       44 Pin PLCC
        Design Check Sum:   72d7bc


15      ++++++++++++++++++++++++++
        | Utilization Information |
        ++++++++++++++++++++++++++
        Utilized cells (no buffers):          83 of      96  (86.5%)
        Utilized cells (buffered):            84 of      96  (87.5%)
20      Input only cells:                      0 of       6  (0.0%)
        Clock only cells:                      0 of       2  (0.0%)
        Bi directional cells:                  7 of      32  (21.9%)
        Routing resources:                  1452 of    5824  (24.9%)
        ViaLink resources:                  1292 of  102664  (1.3%)
25


        ++++++++++++++++++
        | Timing Results |
        ++++++++++++++++++
30
        Summary:

        Clock                 Frequency            Setup Time           Clock to Out
        ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
35      clock                 40 MHz / 24.7 ns       6.7 ns               15.3 ns


        ++++++++++++++++++++++++++++++
        | Tools run on design simul1 |
40      ++++++++++++++++++++++++++++++
        partdef         4.0
        design          3.0
        logic optimizer 7.11    Mode=Quality Goal=Speed Level=2 IgnorePack=FALSE Utilizatio
        placer          7.11    Seed=42 Mode=Quality
45      router          7.11    Seed=42
        delay modeler   7.11    Mode=Commercial Corner=Nominal SpeedGrade=2 LowPower=FALSE
        back annotation 7.11
        verifier        7.11    Strip=TRUE
        sequencer       7.11
50


        +++++++++++++
        | Pin Table |
        +++++++++++++
55      Pin # Pad Name                    Net Name                      PinType   Fixed
        ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
            1 GND                                                                   Y
            2 I_9                         tc_400hz                      OUTPUT    Y
            3 NU (GND)
60          4 NU (GND)
            5 NU (GND)
            6 NU (GND)
            7 NU (GND)
            8 NU (GND)
65          9 NU (GND)
           10 NU (Connect to Vcc or Gnd)
           11 NU (Connect to Vcc or Gnd)
           12 VCC                                                                   Y
```

```
        13 NU (Connect to Vcc or Gnd)
        14 NU (Connect to Vcc or Gnd)
        15 NU (GND)
        16 NU (GND)
        17 NU (GND)
        18 NU (GND)
        19 NU (GND)
        20 NU (GND)
        21 NU (GND)
        22 NU (GND)
                                                                          Y
        23 GND
        24 I_3                          clock                 INPUT       Y
        25 NU (GND)
        26 NU (GND)
        27 NU (GND)
        28 NU (GND)
        29 NU (GND)
        30 NU (GND)
        31 NU (GND)
        32 NU (Connect to Vcc or Gnd)
        33 NU (Connect to Vcc or Gnd)
                                                                          Y
        34 VCC
        35 NU (Connect to Vcc or Gnd)
        36 NU (Connect to Vcc or Gnd)
        37 I_26                         pls2u_1hz             OUTPUT      Y
        38 NU (GND)
        39 NU (GND)
        40 I_18                         del_400hz             OUTPUT      Y
        41 I_14                         tc_1hz                OUTPUT      Y
        42 NU (GND)
        43 tc_p                         tc                    OUTPUT      N
        44 I_4                          clear                 INPUT       Y


    +++++++++++++++++++++
    | Fixed Flip Flops |
    +++++++++++++++++++++
    None



    +++++++++++++++++++++++++++++++++++
    | Nets Removed by Technology Mapper |
    +++++++++++++++++++++++++++++++++++
    Net N_24
    Net N_26
    Net I_6.tc_4
    Net I_8.tc_4
    Net I_15.tc_4
    Net I_22.un5_i[4]
    Net I_8.un5_i[12]
    Net I_8.un5_i[11]
    Net I_8.un5_i[13]
    Net I_8.un5_i[8]
    Net I_8.un5_i[7]
    Net I_8.un5_i[5]
    Net I_8.un5_i[2]
    Net I_6.un5_i[22]
    Net I_6.un5_i[20]
    Net I_6.un5_i[19]
    Net I_6.un5_i[17]
    Net N_1
    Net N_2
    Net N_3
    Net N_5


    ++++++++++  The end of report file  ++++++++++
```


6 I/O
5 I/O
4 I/O
3 I/O
2 I/O tc_400hz
1 GND
44 I/O clear
43 I/O tc
42 I/O
41 I/O tc_1hz
40 I/O del_400hz
7 I/O
8 I/O
9 I/O
10 Input
11 I/CLK
12 VCC
13 input
14 Input
15 I/O
16 I/O
17 I/O
39 I/O
38 I/O
37 I/O pls2u_1hz
36 Input
35 Input
34 VCC
33 I/CLK
32 Input
31 I/O
30 I/O
29 I/O
18 I/O
19 I/O
20 I/O
21 I/O
22 I/O
23 GND
24 I/O clock
25 I/O
26 I/O
27 I/O
28 I/O
QuickLogic
pASIC
QL8X12B-2PL44C


U.S. Army, SBCCOM
Laser Standoff Detection Team
Raphael P. Moon
SIMUL2
SIMUL2
SIMUL2
10/21/99
3:36:20 PM
PLS2U
COUNT5
DEL6U
DEL33U
MUX2x0
DFFC
DFF
INV
BUFF
INPAD
OUTPAD
clock
clear
select
delay6u
pls2u_200hz
in_del_400hz
in_tc_1hz

APPENDIX A

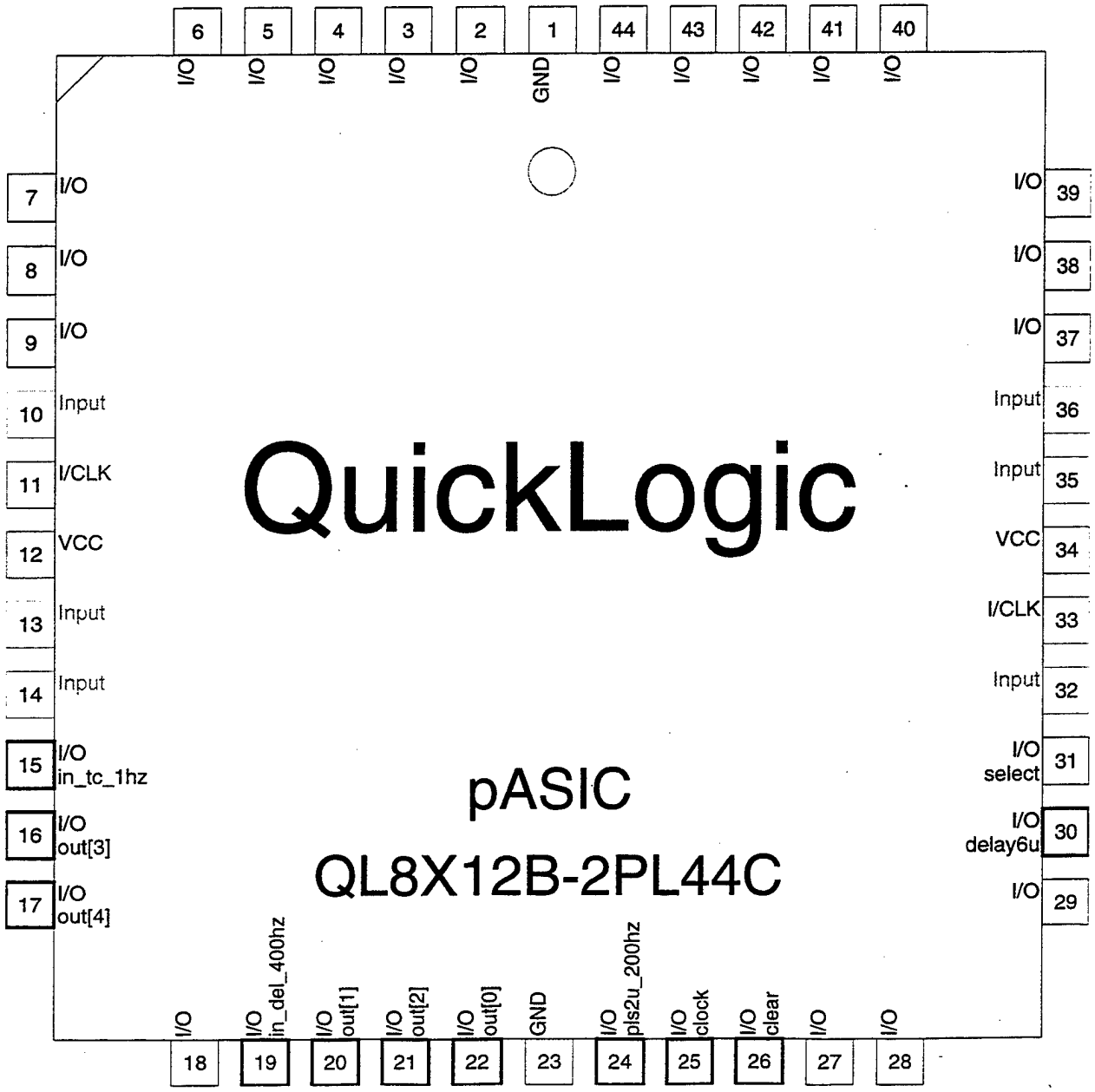
```
//--------------------------------------------------------------------------------
//
// File name    :  C:\pasic\design\moonwork\lidartest\COUNT5.v
// ------------------------------------------------------------------------------
// Revision History :
// ------------------------------------------------------------------------------
//   Ver  :| Author            :| Mod. Date :|
//   v1.0  | Raphael P. Moon   :| 3/29/00   :|


/*Using 400hz clock, and 5 bit counter to make 200hz pulses
and 16 inputs trig. to the decoder.*/

module count5(q,load, clk, clr, tc);
output [4:0] q;
output tc;
input load, clk, clr;
reg[4:0] q;
reg tc;

always@(posedge clr or posedge load or posedge clk)
    begin
        if(clr)
            q=5'b11111;
        else
            begin
                if(load)
                    q=5'b11111;
                else
                    q=q-1;
                        begin
                            if(q==5'b1)
                                tc=1'b1;
                            else
                                tc=1'b0;
                        end
            end
    end
endmodule
```

```
//--------------------------------------------------------------------------
//
// File name    :  C:\pasic\design\moonwork\lidartest\DEL6U.v
// ------------------------------------------------------------------------
// Revision History :
// ------------------------------------------------------------------------
//   Ver  :| Author            :| Mod. Date :|
//   v1.0  | Raphael P. Moon   :| 3/29/00   :| -------------------------


/*Using 10 Mhz clock, and 7 bit counter to make 6.7usec pulse.*/

module del6u(q,load, clk, clr, tc);
output [6:0] q;
output tc;
input load, clk, clr;
reg[6:0] q;
reg tc;

always@(posedge clr or posedge load or posedge clk)
    begin
        if(clr)
            q=7'b1000011;
        else
            begin
                if(load)
                    q=7'b1000011;
                else
                    q=q-1;
                        begin
                            if(q==7'b1)
                                tc=1'b1;
                            else
                                tc=1'b0;
                        end
            end
    end
endmodule
```

```
//--------------------------------------------------------------------------
//
// File name    :  C:\pasic\design\moonwork\lidartest\DEL33U.v
// ------------------------------------------------------------------------
// Revision History :
// ------------------------------------------------------------------------
//   Ver  :| Author            :| Mod. Date :|    Changes Made:
//   v1.0  | Raphael P. Moon   :| 3/29/00   :| Automatically Generated
// ------------------------------------------------------------------------


/*Using 10 Mhz clock, and 9 bit counter to make33.33usec pulse.*/

module del33u(q,load, clk, clr, tc);
output [8:0] q;
output tc;
input load, clk, clr;
reg[8:0] q;
reg tc;

always@(posedge clr or posedge load or posedge clk)
    begin
        if(clr)
            q=9'b101001101;
        else
            begin
                if(load)
                    q=9'b101001101;
                else
                    q=q-1;
                        begin
                            if(q==9'b1)
                                tc=1'b1;
                            else
                                tc=1'b0;
                        end
            end
    end
endmodule
```

```
++++++++++++++++++++++
| Design Information |
++++++++++++++++++++++
Design:             simul2
SpDE Version:       SpDE 8.2
Report Generated:   Thu Mar 30 09:37:32 2000
CHIP Last Updated:  Wed Oct 27 13:02:10 1999
Part Type:          p8x12b
Speed Grade:        2
Operating Range:    Commercial
Package Type:       44 Pin PLCC
Design Check Sum:   637163


++++++++++++++++++++++++++
| Utilization Information |
++++++++++++++++++++++++++
Utilized cells (no buffers):          51 of      96  (53.1%)
Utilized cells (buffered):            51 of      96  (53.1%)
Input only cells:                      0 of       6  (0.0%)
Clock only cells:                      0 of       2  (0.0%)
Bi directional cells:                 12 of      32  (37.5%)
Routing resources:                   912 of    5824  (15.7%)
ViaLink resources:                   806 of   86164  (0.9%)


++++++++++++++++++
| Timing Results |
++++++++++++++++++

Summary:

Longest Pad to Pad: 7.1 ns (select -- delay6u)

Clock                                Frequency       Setup Time      Clock to Out
+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
clock                              75 MHz / 13.3 ns      5.9 ns           N/A
in_del_400hz                       76 MHz / 13.1 ns      9.2 ns         10.4 ns
in_tc_1hz                            N/A                  N/A             N/A


++++++++++++++++++++++++++++++
| Tools run on design simul2 |
++++++++++++++++++++++++++++++
partdef         4.0
design          3.0
logic optimizer 8.0     Mode=Quality Goal=Speed Level=2 IgnorePack=FALSE Utilizatio
placer          8.0     Seed=42 Mode=Quality
router          8.0     Seed=42
delay modeler   8.0     Mode=Commercial Corner=Nominal SpeedGrade=2 LowPower=FALSE
back annotation 8.0
verifier        8.2     Strip=TRUE
sequencer       8.0


+++++++++++++
| Pin Table |
+++++++++++++
Pin # Pad Name                      Net Name                        PinType   Fixed
+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
    1 GND                                                                       Y
    2 NU (GND)
    3 NU (GND)
    4 NU (GND)
    5 NU (GND)
    6 NU (GND)
    7 NU (GND)
    8 NU (GND)
```

```
          9 NU (GND)
70        10 NU (Connect to Vcc or Gnd)
          11 NU (Connect to Vcc or Gnd)
          12 VCC                                                          Y
          13 NU (Connect to Vcc or Gnd)
          14 NU (Connect to Vcc or Gnd)
75        15 I_2                          in_tc_1hz          INPUT        Y
          16 I_17                         out[3]             OUTPUT       Y
          17 I_14                         out[4]             OUTPUT       Y
          18 NU (GND)
          19 I_3                          in_del_400hz       INPUT        Y
80        20 I_15                         out[1]             OUTPUT       Y
          21 I_16                         out[2]             OUTPUT       Y
          22 I_13                         out[0]             OUTPUT       Y
          23 GND                                                          Y
          24 I_12                         pls2u_200hz        OUTPUT       Y
85        25 I_5                          clock              INPUT        Y
          26 I_4                          clear              INPUT        Y
          27 NU (GND)
          28 NU (GND)
          29 NU (GND)
90        30 I_22                         delay6u            OUTPUT       Y
          31 I_29                         select             INPUT        N
          32 NU (Connect to Vcc or Gnd)
          33 NU (Connect to Vcc or Gnd)
          34 VCC                                                          Y
95        35 NU (Connect to Vcc or Gnd)
          36 NU (Connect to Vcc or Gnd)
          37 NU (GND)
          38 NU (GND)
          39 NU (GND)
100       40 NU (GND)
          41 NU (GND)
          42 NU (GND)
          43 NU (GND)
          44 NU (GND)
105

      ++++++++++++++++++++
      | Fixed Flip Flops |
      ++++++++++++++++++++
110   None


      ++++++++++++++++++++
      | Fixed RAM cells  |
115   ++++++++++++++++++++
      None



120   ++++++++++++++++++++++++++++++++++++
      | Nets Removed by Technology Mapper |
      ++++++++++++++++++++++++++++++++++++
      Net N_31
      Net I_9.un6_q[0]
125   Net I_11.un6_q[0]
      Net I_21.un6_q[0]
      Net I_21.tc10
      Net I_28.un6_q[0]
      Net I_28.tc10
130   Net I_11.un6_q_i_1[2]
      Net I_9.un6_q_i_1[2]
      Net I_28.un6_q_i_1[6]
      Net I_28.un6_q_i_1[7]
      Net N_97
135   Net N_99
      Net N_101
```


6 I/O
5 I/O
4 I/O
3 I/O
2 I/O
1 GND
44 I/O
43 I/O
42 I/O
41 I/O
40 I/O
7 I/O
8 I/O
9 I/O
10 Input
11 I/CLK
12 VCC
13 Input
14 Input
15 I/O in_tc_1hz
16 I/O out[3]
17 I/O out[4]
39 I/O
38 I/O
37 I/O
36 Input
35 Input
34 VCC
33 I/CLK
32 Input
31 I/O select
30 I/O delay6u
29 I/O
QuickLogic
pASIC
QL8X12B-2PL44C
18 I/O
19 I/O in_del_400hz
20 I/O out[1]
21 I/O out[2]
22 I/O out[0]
23 GND
24 I/O pls2u_200hz
25 I/O clock
26 I/O clear
27 I/O
28 I/O

APPENDIX B

HP BASIC PROGRAM "RESISTOR.VAL"

```
29 Mar 2000
10:34:41

10     ! PROGRAM "RESISTOR.VAL"
20     ! 9-28-99  N.GREEN REV. 1-13-00
30     ! THIS PROGRAM CALCULATES 15 RESISTOR VALUES TO PRODUCE 15 LINEAR GAIN STEPS
40     ! TO GENERATE OUTPUT AMPLIFIER VOLTAGES FROM 18mV TO 1.8 VOLTS. SUPPLY
41     ! VOLTAGE MEASURED AS 5.16 VOLTS
43     ! Eo=OUTPUT VOLTAGE
44     ! Ga=LINEAR VOLTAGE GAIN
45     ! Db=dB VOLTAGE GAIN
46     ! Ec=AMPLIFIER CONTROL VOLTAGE
47     ! Re=SERIES RESISTOR
48     !
49    PRINTER IS 26
50    PRINT TAB(15);"AGC TEST SET RESISTOR VALUES   "&DATE$(TIMEDATE)
51    PRINT ""
52    PRINT ""
53    PRINT "OUTPUT VOLTAGE";TAB(18);"CONTROL VOLTAGE";TAB(35);"LINEAR GAIN";
54    PRINT TAB(50);"DB GAIN";TAB(64);"RESISTOR VALUE"
56    PRINT ""
57    FOR N=0 TO 14 STEP 1
60    Eo=(1.8E-2)*1.3895^N
70    Ga=Eo/1.8E-2
71    Db=(LGT(Ga))*20
72    Ec=((Db-20)/40)+.5
73    IF Ec>0 THEN
75    Re=(5.1E+3/Ec)-1.E+3
76    ELSE
77    Re=1.E+6
79    END IF
80    Ga=DROUND(Ga,4)
82    Eo=DROUND(Eo,4)
83    Re=DROUND(Re,4)
84    Ec=DROUND(Ec,4)
85    Db=DROUND(Db,4)
86    Re$=VAL$(Re)
87    Ec$=VAL$(Ec)
88    Ga$=VAL$(Ga)
89    Db$=VAL$(Db)
90    Eo$=VAL$(Eo)
91    PRINT Eo$;TAB(18);Ec$;TAB(35);Ga$;TAB(50);Db$;TAB(64);Re$
93    NEXT N
94    PRINT CHR$(12)
95    PRINTER IS 1
96    END
```

AGC TEST SET RESISTOR VALUES 29 Mar 2000

OUTPUT VOLTAGE	CONTROL VOLTAGE	LINEAR GAIN	DB GAIN	RESISTOR VALUE
.018	0	1	0	1.E+6
.02501	.07143	1.39	2.857	70400
.03475	.1429	1.931	5.714	34700
.04829	.2143	2.683	8.572	22800
.0671	.2857	3.728	11.43	16850
.09323	.3571	5.18	14.29	13280
.1295	.4286	7.197	17.14	10900
.18	.5	10	20	9200
.2501	.5714	13.9	22.86	7925
.3475	.6429	19.31	25.71	6933
.4829	.7143	26.83	28.57	6140
.671	.7857	37.28	31.43	5491
.9323	.8572	51.8	34.29	4950
1.295	.9286	71.97	37.14	4492
1.8	1	100	40	4100